Interval Arithmetic Logic Unit for Signal Processing and Control Applications

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Abstract

Many digital signal processing (DSP) and control applications require a small subset of arithmetic operations that must be computed efficiently with high throughput. This allows the required algorithms to be computed in real time. Presently, implementing DSP algorithms using interval arithmetic on general purpose computers as compared to floating point operations results in an increase in computational time of 1.5 to 10 times. To significantly reduce the interval arithmetic computational time would require dedicated hardware. We have proposed a design for an interval based arithmetic logic unit (I-ALU) whose computational time for implementing interval arithmetic operations are equivalent to many digital signal processors.

This design constitutes two independent modules operating in parallel to calculate the lower bound and upper bound of the output interval. The functional unit of the ALU performs the basic fixed point interval arithmetic operations of addition, subtraction and multiplication. In addition, the ALU is optimized to perform the dot product through the multiply-accumulate instruction. Fixed point arithmetic is based on 16-bit twos-complement representation with a 32-bit accumulator. The result is rounded off to either 16 or 24 bit. The I-ALU also provides set operations of union and intersection. Division will be implemented as a shift operation.

This paper will also discuss and compare several performance metrics that are relevant to signal processing and control applications.